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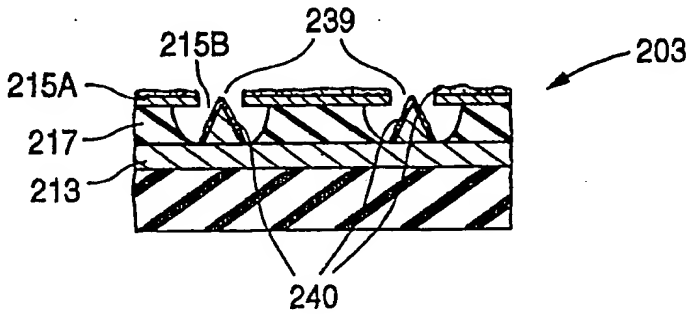
(57) Abstract

A cathode structure (200, 203, 204) suitable for a flat panel display is provided with coated emitters (229, 239, 230). The emitters are formed with material, typically nickel, capable of growing to a high aspect ration. These emitters are then coated with carbon containing material (240, 241) for improving the chemical robustness and reducing the work function. One coating process is a DC plasma deposition process in which acetylene is pumped through a DC plasma reactor (301, 305, 313, and 315) to create a DC plasma for coating the cathode structure. An alternative coating process is to electrically deposit raw carbon–based material onto the surface of the emitters, and subsequently reduce the raw carbon–based material to the carbon containing material. Work function of coated emitters is typically reduced by about 0.8 to 1.0 eV.



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FABRICATION AND STRUCTURE OF ELECTRON EMITTERS COATED WITH MATERIAL SUCH AS CARBON

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to electron emission devices. More specifically, this invention relates to the structure and manufacture of electron emissive elements used in flat panel displays.

Background Art

In a flat panel display, a matrix of electron emitters emit electrons that impinge on a transparent display panel coated with light emitting material such as phosphor. The principles of a flat panel display can be more clearly explained by referring to Figs. 1A, 1B, and 1C (collectively Fig. 1), which illustrate a flat panel display structure.

In Fig. 1A, backplate 120 is provided as a support to which electrically conductive emitter layer 113 is attached. Generally conical electron emitters 116 are formed on emitter layer 113. In Fig. 1B, electron emitters 116 are formed within gate holes 115B, under gate layer 115A. Gate layer 115A is separated from emitter layer 113 by dielectric layer 117. Display panel 118 having light emissive layer 110 and anode layer 111 is situated above, and spaced vertically apart from, gate layer 115A.

Portions of gate layer 115A are provided with sufficiently greater voltage than emitter layer 113 and electron emitters 116 to enable layer 115A to extract electrons from electron emitters 116. Anode layer 111

is at a considerably greater voltage than emitter layer 113 or gate layer 116. As a result, a large fraction of the electrons emitted from electron emitters 116 are extracted by anode layer 111 toward transparent panel 118. With anode layer 111 being quite thin, the electrons pass through anode layer 111 and impinge on the phosphor coating 110 on panel 118, causing light emissive layer 110 to emit light.

Fig. 1C shows a cathode structure 100 for a flat panel display. Emitter layer 113 is divided into mutually insulated emitter rows 114, while gate layer 115A is divided into mutually insulated columns 184. For a black and white display, the overlapping area of a row 114 and a column 184 represents a pixel 130, the smallest element of a picture. For a color display, several (normally three) overlapping row/column areas form a pixel. In order to cause a selected group of emitters 116 to emit electrons thereby to energize a pixel, an appropriate electric field must be created between electron emitters 116 and gate layer 115A. In particular, a voltage must be applied between a selected row 114 and a selected column 184 to place that row 114 at a suitably greater potential than that column 184, thereby causing electron emission from emitters 116 at that row/column intersection. When the voltage between the selected row 114 and the selected column 184 is below a non-zero threshold value, emitters 116 at the row/column intersection do not emit electrons, and the corresponding pixel is not excited.

Referring to Fig. 1C, a complete picture requires the scanning of every row and every column. In order to have the picture appear to be continuous to the human eye, the scanning must be performed at high speed. Thus the voltage between a specific row and column must change in a very short time.

The geometry of rows 114 and columns 184 together with the thickness H and the dielectric constant of dielectric layer 117 determines the crossover capacitance between a row 114 and a column 184. When thickness H is small, the crossover capacitance is large. This capacitance substantially slows down the activation of electron emitters 116, resulting in poor display. Therefore, it is desirable that dielectric layer 117 be thick. When the thickness of dielectric layer 117 increases, the height of electron emitters 116 normally must also increase in order to bring their tips sufficiently close to gate layer 115A to enable layer 115A to extract electrons from them.

A thick dielectric layer also reduces the possibility of short circuiting. During display operation, undesirable conductive paths may be produced through dielectric layer 117 so as to short circuit emitter layer 113 and gate layer 115A. As thickness H (Fig. 1C) of dielectric layer 117 increases, the likelihood of short circuiting gate layer 115A to emitter layer 113 by creating such a conductive path decreases. Further, in Fig. 1A, hollow spaces 119 keep gate layer 115A spaced apart from electron emitters 116. Because gate holes 115B are typically quite small, as little as 80 nm in diameter, a metal particle falling into hollow space 119 may cause short circuiting between gate layer 115A and electron emitters 116. With a thick dielectric layer 117, hollow space 119 would have an elongated profile. A particle falling into hollow space 119 tends to rest within the hollow space and away from gate hole 115B, and thus is less likely to cause short circuiting.

For conical electron emitters with a given aspect ratio (height to base diameter), larger gate holes 115B are required in order to create higher conical electron emitters 116. However, for fine quality picture, it is

desirable to have more electron emitters per unit area. Thus it is desirable to have small gate holes. Small gate holes also give greater field strength at the emitters, resulting in lower applied voltage between rows and columns to achieve a given emission current. High aspect ratio cones allow a thick dielectric layer to be used, thus giving the advantages of reduced cross-over capacitance and greater short protection. Consequently, a higher aspect ratio is desirable for making a better cathode structure.

Certain materials such as nickel can be used to create electron emitters with a high aspect ratio. However, nickel does not have other properties desired for electron emitters. For example, nickel has poor chemical robustness. Also, nickel is easily oxidized. Oxidized nickel emitters have an increased extraction voltage and decreased emission stability.

Nickel has a relatively high work function. Work function is defined as the level of energy necessary to energize an electron to such a level that the electron is emitted from the material. A high work function means that a stronger electric field is required between the electron emitter 116 and corresponding column 184 of gate layer 115A in order to energize the electrons. This stronger electric field translates to a greater column-to-row extraction voltage. A high column-to-row extraction voltage is undesirable because it results in high power consumption and more expensive circuitry.

It is therefore desirable to have electron emitters with a high aspect ratio, good chemical robustness and low work function.

GENERAL DISCLOSURE OF THE INVENTION

In accordance with the present invention, improved electron emitters are provided with high aspect ratios,

good chemical robustness and low work function. Electron emitters are formed with electrically non-insulating material that allows deposition to a high aspect ratio at low deposition temperature. One candidate material for the electron emitters is nickel. Electron emitters so made are coated with surface material that has good chemical robustness and low work function. One candidate for the surface material is carbon. The emitter and surface materials may also be chosen for other desirable electrical or chemical properties. Work function of coated emitters is typically reduced by about 0.8 to 1.0 eV.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a perspective view of a conventional flat panel display.

Fig. 1B is a cross-sectional view of a portion of the conventional flat panel display of Fig. 1A.

Fig. 1C is a perspective view of a cathode structure in the conventional flat panel display of Fig. 1A.

Figs. 2A - 2F are cross-sectional views representing steps in accordance with this invention for fabricating a cathode structure with electron emitters.

Fig. 3 is a schematic view of a DC plasma reactor used for coating a cathode structure in accordance with the present invention.

Fig. 4 is a process diagram used for coating a cathode structure in accordance with the present invention.

Fig. 5 is a cross-sectional view of a flat panel display in accordance with the present invention using the electron emitters of Fig. 2E.

Fig. 6A is a schematic view of an apparatus for coating a cathode structure using electrochemical deposition.

Figs. 6B-6F are cross-sectional views of cathode structures where the emitters are coated with carbon containing material using electrochemical deposition.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Herein, the term "electrically insulating" (or "dielectric") generally applies to materials having a resistivity greater than 10^{10} ohm-cm. The term "electrically non-insulating" thus refers to materials having a resistivity below 10^{10} ohm-cm. Electrically non-insulating materials are divided into (a) electrically conductive materials for which the resistivity is less than 1 ohm-cm and (b) electrically resistive materials for which the resistivity is in the range of 1 ohm-cm to 10^{10} ohm-cm. These categories are determined at an electric field of no more than 1 volt/μm.

Examples of electrically conductive materials (or electrical conductors) are metals, metal-semiconductor compounds (such as metal silicides), and metal-semiconductor eutectics. Electrically conductive materials also include semiconductors doped (n-type or p-type) to a moderate or high level. Electrically resistive materials include intrinsic and lightly doped (n-type or p-type) semiconductors. Further examples of electrically resistive materials are metal-insulator composites, graphite, amorphous carbon, and modified (e.g., lightly doped or laser-modified) diamond.

Figs. 2A, 2B, 2C, 2D, and 2E (collectively Fig. 2) show one process for manufacturing a flat panel display according to the invention's teachings. Electrically non-insulating emitter layer 213 patterned into emitter rows is provided on electrically insulating backplate

220. Emitter (or cathode) layer 213 is typically formed with metal, such as aluminum or nickel, covered by electrically resistive material, such as lightly doped polycrystalline silicon, a silicon carbon nitrogen compound, or cermet (ceramic with embedded metal particles). In Fig. 2A, dielectric layer 217, typically silicon oxide, is deposited on emitter layer 213. On top of dielectric layer 217 is deposited electrically non-insulating gate material, typically a metal, to form gate layer 215A, thereby providing sub-structure 201.

Gate holes 215B are selectively etched through gate layer 215A. International Application PCT/US97/09197, filed 5 June 1997, discloses a method for etching gate holes using electrophoretic or dielectrophoretic particle deposition. U.S. Patents 5,462,467 and 5,564,959 disclose methods for making gate holes using charged-particle tracks. The contents of these three documents are incorporated by reference herein.

After gate holes 215B are formed, structure 201 is cleaned. Structure 201 is then subjected to another etchant to remove exposed parts of dielectric material 217 and form hollow spaces 219.

In Fig. 2B, liftoff layer 242 is then deposited on gate layer 215A. The material for liftoff layer 242 is chosen so that it can be selectively etched away with respect to gate layer 215A, dielectric layer 217 and lower electrically non-insulating emitter region 213. Liftoff layer 242 is deposited on the top of gate layer 215A at an angle α relative to the upper surface of gate layer 215A. Angle α is so chosen that the liftoff material will not be deposited on the exposed areas of emitter layer 213 within hollow spaces 219. Angle α depends on the geometry of hollow spaces 219. For a thicker dielectric layer 217, angle α can be larger,

and vice versa. Angle α is also dependent on the geometry of gate holes 215B. For a larger gate hole 215B, angle α can be smaller, and vice versa.

In Fig. 2C, electrically non-insulating emitter material is deposited, typically by physical vapor deposition, on top of the structure in a direction generally perpendicular to the upper surface of gate layer 215A. This emitter material accumulates on liftoff layer 242 and passes through gate holes 215B to accumulate on lower electrically non-insulating emitter layer 213. Openings 246 through which emitter material enters hollow spaces 219 progressively close as the emitter material accumulates on electrically non-insulating emitter layer 213. The deposition is performed until openings 246 are fully closed. As a result the emitter material accumulates in hollow spaces 219 to form generally conical electron emitters 229. A continuous layer 244 of the emitter material is simultaneously formed on liftoff layer 242.

Liftoff layer 242 is then removed with a suitable etchant. During the removal of liftoff layer 242, excess emitter material layer 244 is lifted off. Fig. 2D shows the resultant cathode structure 200 with electron emitters 229. Each electron emitter 229 is concentric with a corresponding gate hole 215B.

In an alternative embodiment, the step of depositing liftoff layer 242 is eliminated. Electrically non-insulating emitter material is deposited on top of structure 201 directly to form electron emitters. International Application PCT/US97/02973, filed 5 March 1997, discloses the technology and is herein incorporated by reference.

The emitter material is normally a metal such as nickel. Openings 246 close at different speeds depending on the chemical composition of the emitter material used. When openings 246 close faster,

electron emitters 229 have a lower aspect ratio. As used here, "aspect ratio" means the height of an emitter divided by its maximum diameter. The maximum diameter of a conical emitter occurs at its base. Accordingly, the aspect ratio of each conical emitter 229 is its height divided by its base diameter. For emitters 229 with a fixed base diameter, a lower aspect ratio means that they have a lesser height, while a higher aspect ratio means that they have a greater height.

The speed at which openings 246 close determines the aspect ratio of emitters 229. When openings 246 close faster, emitters 229 have a low aspect ratio, and vice versa.

In one embodiment where physical vapor deposition is employed to deposit emitters 229, increasing the deposition temperature causes openings 246 to close slower, resulting in a higher aspect ratio for emitters 229. At high temperature, however, physical vapor deposition techniques become more complicated. Therefore, a low temperature physical vapor deposition process is typically employed for making emitters 229.

Certain metals, such as nickel, have a unique property that allows them to deposit through suitable deposition openings at a high aspect ratio at low temperature. At 25°C (approximately room temperature), the aspect ratio of nickel emitters is between 1.5 and 2.0. With certain other metals, the aspect ratio is considerably lower. Molybdenum emitters, for example, can be deposited to an aspect ratio of 0.9-1.0 at 25°C. To obtain an aspect ratio of about 1.0 with metal other than nickel or molybdenum, a temperature of 400°C to 600°C is often required. Generally, materials that can be deposited to an aspect ratio of at least 1.2 using physical vapor deposition at room temperature (25°C) are highly desirable.

Other techniques such as electroplating as disclosed in U.S. Patents 5,462,467 and 5,564,959 can also be used for making electron emitters, particularly when they are filamentary in shape. For example, with gate openings 215B present in gate layer 215A, dielectric layer 217 can be anisotropically etched through gate openings 215B, to form largely straight openings through dielectric layer 217 down to emitter layer 213. Emitter metal can be electroplated (electrochemically deposited) into the dielectric openings to form metal filaments up nearly to gate openings 215B. The dielectric openings can be optionally widened using an isotropic etchant, and the filaments can be sharpened to form filamentary electron emitters.

The benefits of surface coating, i.e., reduced work function and improved chemical robustness, do not depend on the method used for making the emitters. Thus, as long as emitters 229 are coated with material with a lower work function according to this invention, variations in method for forming emitters 229 are within the scope of the present invention.

Fig. 2D illustrates the resultant cathode structure 200 with high aspect ratio nickel electron emitters 229. Electrically non-insulating material other than nickel, such as palladium and platinum, may also be used for making emitters 229. Nickel, palladium, and platinum may not have the desired work function and chemical robustness as required for electron emitters. For example, palladium has a work function of about 5.12 eV, while nickel has a work function of about 5.15 eV. Platinum has a work function of about 5.67 eV. Thus, nickel, palladium, and platinum all have work function greater than 5.00 eV, in contrast, molybdenum has a work function of about 4.60 eV. For non-coated emitters made of

material with a work function higher than 5.00 eV, such as palladium, platinum, or nickel, a high operating voltage is often required to cause electron emission. Operating voltage is defined as the voltage between gate layer 215A and emitter layer 213 for causing an electron emission of 0.2 nA per emitter 239 (Fig. 2E).

Another problem with some emitter material is the poor chemical robustness. Material with poor chemical robustness tend to chemically react with elements the emitters come into contact with, such as oxygen and water. When such material is used for making emitters, a high vacuum must be maintained within the flat panel display, resulting in higher cost.

In accordance with the present invention, superior emitter performance is obtained by coating emitters 229 with carbon containing material. The carbon content of the coating material is normally at least 33 1/3 atomic percent, typically at least 50 atomic percent, preferably at least 80 atomic percent. Fig. 2E shows a cathode structure 203 in which electron emitters 239 and gate layer 215A have a layer of carbon containing material 240 thereon. Fig. 2F shows a cathode structure 204 with filamentary shaped emitters 230 coated with carbon containing material 241.

Metal emitter materials, such as tantalum, titanium, rhodium, chromium, and vanadium, can similarly benefit from coating with carbon containing material.

Coatings of 5 to 100 angstroms in thickness have been provided on nickel emitters. The thickness of the carbon containing material varies depending on the conditions of the coating process. In one embodiment of the present invention, a coating of 20 to 70 angstroms was found to give good results, even though all coating thicknesses in the 5-to-100 angstrom range were found to be satisfactory.

Comparisons were made on the electron emissive properties of coated nickel emitters and non-coated nickel emitters. The first comparison involved the operating voltage of the emitters. With non-coated nickel emitters, the operating voltage was about 30 to 35 V. The operating voltage for coated nickel emitters was about 20 V. Thus, with carbon containing layer, the operating voltage decreased by 10 to 15 V.

The work functions of coated and non-coated nickel are measured by the contact potential difference method. For nickel not coated with carbon containing layer, the work function is 5.15 eV. The work function of coated nickel emitters is between 4.15 to 4.35 eV. Thus, for nickel emitters, the reduction in work function as a result of coating with a carbon containing layer is determined to be 0.8 to 1.0 eV.

The electron emission uniformity of coated emitters 239 has been measured. In comparison with non-coated nickel emitters 229, coated nickel emitters 239 gave as good, or better, electron emission uniformity.

When depositing carbon onto metal, carbon may form either a crystalline structure or a non-crystalline structure, depending on the condition of the coating process. Carbon in crystalline form is either diamond or graphite, while non-crystalline carbon is amorphous carbon. Amorphous carbon may contain a substantial amount of hydrogen. Amorphous carbon with a substantial amount of hydrogen and a large sp^3/sp^2 ratio is also called diamond-like carbon. Amorphous carbon is frequently characterized by the sp^3/sp^2 bond ratio. Carbon with a large sp^3/sp^2 ratio and little hydrogen is called tetrahedral amorphous carbon. Graphite and amorphous carbon coatings were found to give better uniformity of electron emission than diamond-like-

carbon coating, which in turn gives better uniformity than diamond coating.

In accordance with the present invention, some hydrogen is usually present in the carbon containing material that coats emitters 229. The minimum atomic percentage of hydrogen in the carbon containing coating is typically one percent. More particularly, the hydrogen content of the carbon containing material is normally 5-50 atomic percent, usually 10-40 atomic percent, and preferably 15-30 atomic percent.

Fig. 3 is a schematic view of a DC plasma reactor used for coating nickel emitters with carbon containing material according to the present invention. The carbon containing material consists primarily of carbon mixed with hydrogen.

Reactor chamber 301 of the DC plasma reactor is a 20-cm conflat flange with a 15-cm inner chamber diameter. Chamber 301 is a cool-wall vacuum chamber pumped by a 60 liter-per-second turbo pump 313. Turbo pump 313 is backed by a mechanical pump 315. Plasma gas is provided to reactor chamber 301 through gas inlets 309. Anode 305 is a piece of molybdenum foil. Structure 200 is placed on an electrically insulating macor piece 321. The electrically insulating macor piece sits on a molybdenum plate 329 which in turn sits on an inductive graphite heater 333. Both molybdenum plate 329 and graphite heater 333 serve as cathode for the DC plasma.

Fig. 4 is a process diagram for coating emitters 229 with carbon containing material according to the invention using the DC plasma reactor shown in Fig. 3. In step 405, reactor chamber 301, anode 305 and cathode 329 are cleaned with hydrogen plasma. During the cleaning stage, cathode structure 200 is not installed in chamber 301. Reactor chamber 301 is sealed with a copper gasket and evacuated to 1×10^{-3} torr using turbo

pump 313. Purified hydrogen (99.9%) is pumped through chamber 301 using mechanical pump 315. A 500 V DC voltage is supplied to anode 305 and graphite heater 333 to generate a DC hydrogen plasma for cleaning. The plasma is run for 15 to 30 minutes. The hydrogen plasma removes carbon deposits on anode 305 and cathode 329 from previous carbon coating runs. Chamber 301 is pumped to 0.3 to 1 torr vacuum. The hydrogen is then pumped out of chamber 301.

In step 407, chamber 301 is opened, and structure 200 is loaded immediately into chamber 301. Dry nitrogen is quickly released into chamber 301 to remove extrinsic particles that have accumulated on structure 200. Chamber 301 is then sealed and pumped to below 5 x 10^{-4} torr vacuum using turbo pump 313.

In step 409, structure 200 is cleaned with hydrogen plasma while situated within reactor chamber 301. Hydrogen is pumped into chamber 301 and the inductive heater 333 is turned on and set to 200°C - 250°C, the desired carbon deposition temperature. Hydrogen gas is then pumped into chamber 301 to clean cathode structure 200. The conditions for the plasma are 100-sccm flow rate, 300 mtorr, and 500 V DC. Mechanical pump 315 only is used. Hydrogen plasma is run for 30 minutes during which structure 200 is heated to the deposition temperature of 250°C. In other embodiments, the deposition temperature may vary from 100°C to 500°C.

During step 411, the DC voltage is turned off, 99.6% pure acetylene at 15 sccm is pumped through chamber 301 for 10 to 30 minutes for gas exchange and temperature stabilization.

During step 413, the 500 V DC power is applied to anode 305 and graphite heater 333 to generate DC plasma. Although a 500 V DC voltage is used here, in other embodiments a DC voltage of between 300 V and 500

V can be used. The plasma current is monitored, and structure 200 is coated for 20 to 30 minutes. Carbon containing material is deposited on the exposed surface of structure 200, including the exposed area of emitter layer 213 and the surface of emitters 229, dielectric layer 217, and gate layer 215. Chamber 301 is kept at a vacuum level of 0.1 torr. Mechanical pump 315 only is used.

The plasma gas is then removed from chamber 301. During step 415, structure 200 is allowed to cool to room temperature in the vacuum within chamber 301 for 2 hours. In another embodiment, structure 200 is allowed to cool within chamber 301 for 1 hour.

The crystalline structure and thickness of the carbon coating depend on the voltage, pressure and content of the plasma, and the coating time. For example, the longer the time that the DC acetylene plasma is present and the acetylene gas is flowed through chamber 301 in step 413, the thicker the resulting carbon containing layer.

With the process described above, the resulting carbon containing layer is primarily amorphous carbon mixed with some hydrogen. We believe the sp^3/sp^2 bond ratio is greater than one. The carbon content of the carbon containing material is more than 33 1/3 atomic percent. With the variation in the carbon deposition conditions, the carbon content may also change. The carbon content can regularly be greater than 50 atomic percent, and under closely controlled deposition conditions, the carbon content can be 80 atomic percent or more. The hydrogen content is normally 1-20 atomic percent.

As explained above, electrically non-insulating carbon containing material is deposited on the exposed surface of structure 200, including the surface of gate layer 215 and the exposed area of emitter layer 213.

In one embodiment of this invention, the gate layer is divided into mutually insulated columns for pixel addressing. As used herein, "mutually insulated" means to be spaced apart by vacuum, air or electrically insulating material, or otherwise not in direct contact with each other. Alternatively, a separate electrically non-insulating addressing layer is used for addressing purposes. The addressing layer can either be formed over the gate layer, or between the gate layer and dielectric layer 217. When a separate addressing layer is used, it is divided into mutually insulated columns together with the gate layer thus to accomplish pixel addressing.

Even though a layer of carbon containing material covers the entire upper surface of gate layer 215, there is little danger of electrically shorting the neighboring columns. The carbon containing layer has low conductivity, and the thickness of the carbon layer is small. Thus the resulting conductance through the carbon containing layer from column to column is negligible.

Fig. 5 shows a flat panel display 500 in accordance with the present invention using coated nickel electron emitters 239. Display panel 218 with light emissive layer 210 and anode layer 211 is situated above, and spaced vertically from, gate layer 215A. Light emissive layer 210 is typically a layer of phosphor situated over display panel 218. Note that a carbon containing layer is deposited over emitters 239, gate layer 215A and dielectric layer 217. For addressing purposes, gate layer 215A is divided into columns while emitter layer 213 is divided into rows. Alternatively, gate layer 215A can be divided into rows while emitter layer 213 can be divided into columns. An insulated column or row of the gate layer is called

a gate line, while an insulated row or columns of the emitter layer is called an emitter line.

Flat panel display 500 has improved electron emission uniformity with reduced operating voltage in comparison to conventional flat panel displays.

Fig. 6A illustrates another method for electrochemically coating electron emitters 229 with carbon containing material. A cathode structure is submerged in a suitable electrolytic solution containing raw carbon-based material in the form of a polymer or monomer. The carbon content in the raw carbon-based monomer and straight-chain polymers is normally no more than 50 atomic percent, commonly less than 33 1/3 atomic percent. The raw carbon-based material is subsequently processed to increase the carbon content to make the carbon containing material.

An electric field is created in the electrolytic solution. The polymer or monomer material is deposited on emitters 229, one of which is shown in Fig. 6A, through electrolytic deposition. Normally it is easier for the polymer or monomer to reach and deposit on the emitter tip rather than on the lower surface material of emitters 229. As a result, the thickness of the deposit at the tips is normally greater than that in other areas, especially near the bases of emitters 229.

The polymer or monomer can nonetheless be deposited on the lower material of emitters 229, including the material along the peripheries of the emitter bases, and on the exposed area of emitter layer 213. Several factors determine whether or not the polymer or monomer deposits on the lower material of emitters 229 and the exposed area of emitter layer 213. Those factors include the size of hollow spaces 319, the deposition temperature, the surface tension of the electrolytic solution relative to emitters 229 and emitter layer 213, and the amount and strength of

surface active wetting agent used, if any. Fig. 6B shows a cathode structure where polymer or monomer is coated on the entire exposed surface of each emitter 229 as well as the exposed area of emitter layer 213. Fig. 6C shows a cathode structure where the entire exposed surface of each emitter 229 is coated with polymer or monomer while the exposed area of the emitter layer 213 is not coated with the polymer or monomer.

The polymer or monomer layer is then suitably treated to produce the desired carbon containing material coating. One process of treatment is pyrolysis. An alternative treating process is a chemical treatment process by which the polymer or monomer layer is modified into a layer of the desired carbon containing material. A suitable chemical treatment process is disclosed in U.S. Patent 5,463,271, the content of which is incorporated by reference herein. The carbon content of the final coating is normally greater than 33 1/3 atomic percent, often greater than 50 atomic percent but, in any event, greater than in the raw carbon-based material.

Figs. 6D and 6E show filamentary shaped emitters coated with carbon containing material using the electrochemical deposition process described above. In Fig. 6D the carbon containing material is coated only on the tip area of emitters 329, while in Fig. 6E the carbon containing material is coated on the entire exposed area of each emitter 329.

The above described coating processes are for illustrative purposes only. For similar coating results, variations can be made to the processes described above. For example, in the plasma coating process, voltages and/or times different from those described above may be employed. Other forms of energy, such as microwaves or radio frequency waves,

may also be used to produce the plasma. These variations do not deviate from the general principles of the invention and are considered within the scope of the invention.

Although this invention has been described in connection with several embodiments and examples, the invention is not limited to the embodiments disclosed, but is capable of various modifications. The invention is only limited by the following claims.

WHAT IS CLAIMED IS:

1. A structure comprising:

a sub-structure;

a plurality of electron emitters situated over said sub-structure, each emitter comprising electrically non-insulating material chosen from nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium; and

a carbon-containing layer coated over each of said electron emitters.

2. A structure comprising:

a sub-structure comprising an electrically non-insulating emitter layer divided into mutually insulated emitter lines;

a plurality of electron emitters situated on said emitter lines, each emitter comprising electrically non-insulating material;

an electrically non-insulating gate layer having an upper surface spaced above said electron emitters, said gate layer having a plurality of gate holes each corresponding to one of said electron emitters, said gate layer being divided into mutually insulated gate lines; and

a carbon-containing layer coated over each of said electron emitters and said gate layer.

3. A structure according to Claim 2, wherein the electrically non-insulating material of said emitters comprises at least one of nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium.

4. A structure comprising:

a sub-structure;

a plurality of electron emitters situated over said sub-structure, each emitter comprising

electrically non-insulating material that can be deposited to an aspect ratio of height to maximum diameter of at least 1.2 at a temperature of 25°C using physical vapor deposition through a deposition opening; and

a carbon-containing layer coated over each of said electron emitters.

5. A structure according to Claim 4, wherein said emitters comprise nickel.

6. A flat panel display structure comprising:

a display panel having an anode layer and a light emissive layer;

a backplate disposed in spaced alignment from said display panel;

an electrically non-insulating emitter layer situated over said backplate;

a plurality of electron emitters situated over said emitter layer, each emitter comprising electrically non-insulating material chosen from nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium; and

a carbon-containing layer coated over each of said electron emitters.

7. A flat panel display structure comprising:

a display panel having an anode layer and a light emissive layer;

a backplate disposed in spaced alignment from said display panel;

an electrically non-insulating emitter layer situated over said backplate, said emitter layer divided into spaced apart emitter lines;

a plurality of electron emitters situated over said emitter lines, each emitter comprising electrically non-insulating material;

an electrically non-insulating gate layer having an upper surface spaced above said electron emitters, said gate layer having a plurality of gate holes each corresponding to one of said electron emitters, said gate layer being divided into mutually insulated gate lines; and

a carbon-containing layer coated over said upper surface of said gate layer and each of said electron emitters.

8. A structure according to Claim 7, wherein the electrically non-insulating material of said emitters comprises at least one of nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium.

9. A flat panel display structure comprising:

a display panel having an anode layer and a light emissive layer;

a backplate disposed in spaced alignment from said display panel;

an electrically non-insulating emitter layer situated over said backplate;

a plurality of electron emitters situated over said emitter layer, each emitter comprising electrically non-insulating material that can be deposited to an aspect ratio of height to maximum diameter of at least 1.2 at a temperature of 25°C using physical vapor deposition through a deposition opening; and

a carbon-containing layer coated over each of said electron emitters.

10. A structure according to Claim 9, wherein said emitters comprise nickel.

11. A structure according to Claim 9, further including a dielectric layer situated above said emitter layer, said dielectric layer having a plurality of dielectric openings, each corresponding to one of said emitters.

12. A structure according to any of Claims 1 - 11, wherein said emitters are generally conical in shape.

13. A structure according to any of Claims 1 - 11, wherein said carbon containing layer consists of at least 33 1/3 atomic percent carbon.

14. A structure according to any of Claims 1 - 11, wherein said carbon containing layer consists of at least 50 atomic percent carbon.

15. A structure according to any of Claims 1 - 11, wherein said carbon containing layer consists of at least 80 atomic percent carbon.

16. A structure according to any of Claims 1 - 11, wherein said carbon-containing layer consists of 5 to 50 atomic percent hydrogen.

17. A structure according to any of Claims 1 - 11, wherein said carbon-containing layer comprises graphite.

18. A structure according to any of Claims 1 - 11, wherein said carbon-containing layer comprises tetrahedral amorphous carbon.

19. A structure according to any of Claims 1 - 11, wherein said carbon-containing layer comprises diamond-like carbon.

20. A structure according to any of Claims 1 - 11, wherein said carbon containing layer is 5 to 100 angstroms in thickness.

21. A structure according to any of Claims 1 - 3 and 6 - 8, wherein said emitters are generally filamentary in shape.

22. A method comprising the steps of:

forming a cathode structure having electron emitters comprising electrically non-insulating material chosen from among nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium, said cathode structure further having a gate layer divided into gate lines; and

coating said emitters with carbon containing material.

23. A method according to Claim 22, wherein the forming step comprises the steps of:

providing a sub-structure; and

providing the emitters over said sub-structure using electroplating.

24. A method comprising the steps of:

forming an emitter layer over a backplate layer;

forming a dielectric layer over said emitter layer;

forming a gate layer over said dielectric layer, said gate layer having an upper surface;

selectively etching holes through said gate layer and said dielectric layer to expose areas of said emitter layer;

forming electron emitters comprising electrically non-insulating material within said holes over said exposed areas of said emitter layer;

dividing said gate layer into mutually insulated gate lines; and

coating said electron emitters and the upper surface of said gate layer with carbon containing material.

25. A method according to Claim 24, wherein the electrically non-insulating material of said emitters comprises at least one of nickel, palladium, platinum, tantalum, titanium, rhodium, chromium, and vanadium.

26. A method comprising the steps of:

forming a cathode structure having electron emitters comprising electrically non-insulating material that can be deposited to an aspect ratio of height to maximum diameter of at least 1.2 at a temperature of 25°C using physical vapor deposition through deposition holes; and

coating said emitters with carbon containing material.

27. A method according to Claim 26, wherein said electrically non-insulating material comprises nickel.

28. A method according to any of Claims 22 and 24 - 27, wherein said emitters are generally conical in shape.

29. A method according to any of Claims 22 - 27, wherein said carbon containing material consists of at least 33 1/3 atomic percent carbon.

30. A method according to any of Claims 22 - 27, wherein said carbon containing material consists of at least 50 atomic percent carbon.

31. A method according to any of Claims 22 - 27, wherein said carbon containing material consists of at least 80 atomic percent carbon.

32. A method according to any of Claims 22 - 27, wherein the coating step comprises subjecting said structure to a DC aceylene plasma comprising carbon.

33. A method according to Claim 32, wherein the carbon in the DC plasma comes at least partly from acetylene in the plasma.

34. A method according to any of Claims 22 - 27, wherein the coating step comprises the steps of:

electrochemically depositing raw carbon-based material; and

reducing said raw carbon-based material to form said carbon containing material.

35. A method according to Claim 34, wherein said raw carbon-based material comprises a polymer.

36. A method according to Claim 34, wherein said raw carbon-based material comprises a monomer.

37. A method according to Claim 34, wherein the reducing step increases the carbon content of said raw

carbon-based material to produce said carbon containing material.

38. A method according to Claim 34, wherein the reducing step comprises heating said raw carbon-based material such that said raw carbon-based material is reduced to said carbon containing material through pyrolysis.

39. A method according to Claim 34, wherein the reducing step comprises chemically treating said raw carbon-based material.

40. A method according to any of Claims 22 - 27, wherein the coating step comprises the steps of:

cleaning a DC plasma reactor chamber;

loading said cathode structure into said chamber; and

pumping a DC plasma gas through said chamber to coat said emitters with carbon containing material.

41. A method according to any of Claims 22 - 27, further including, after the pumping step, the step of allowing said cathode structure to cool in said reactor chamber.

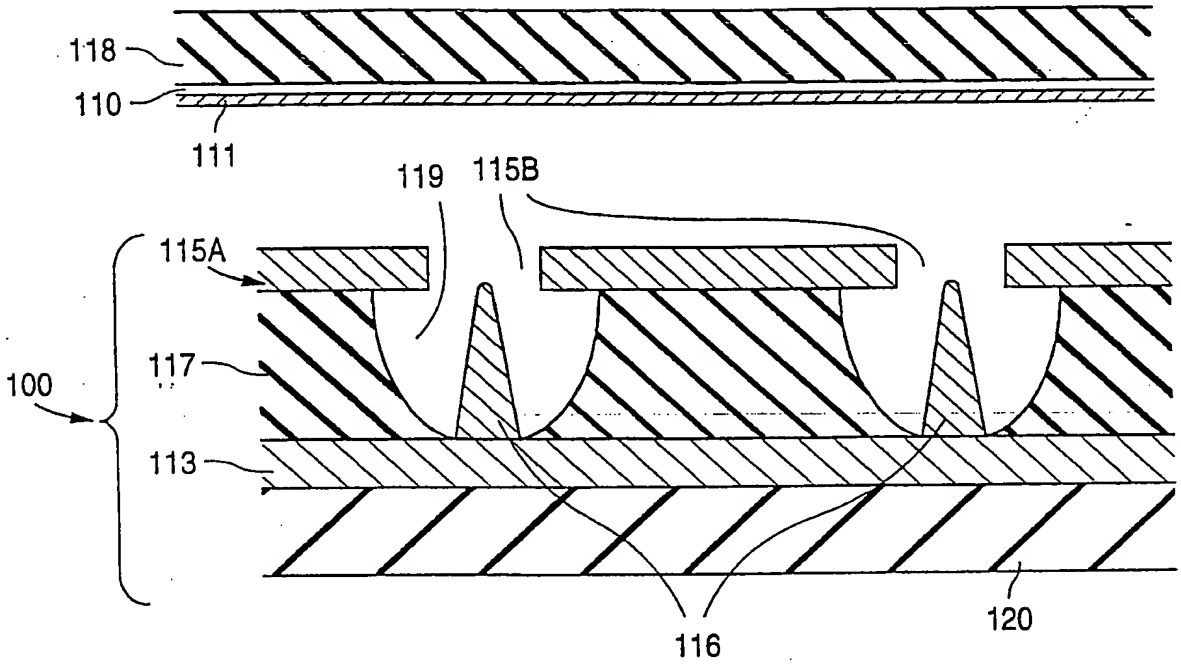

Fig. 1A
Prior Art

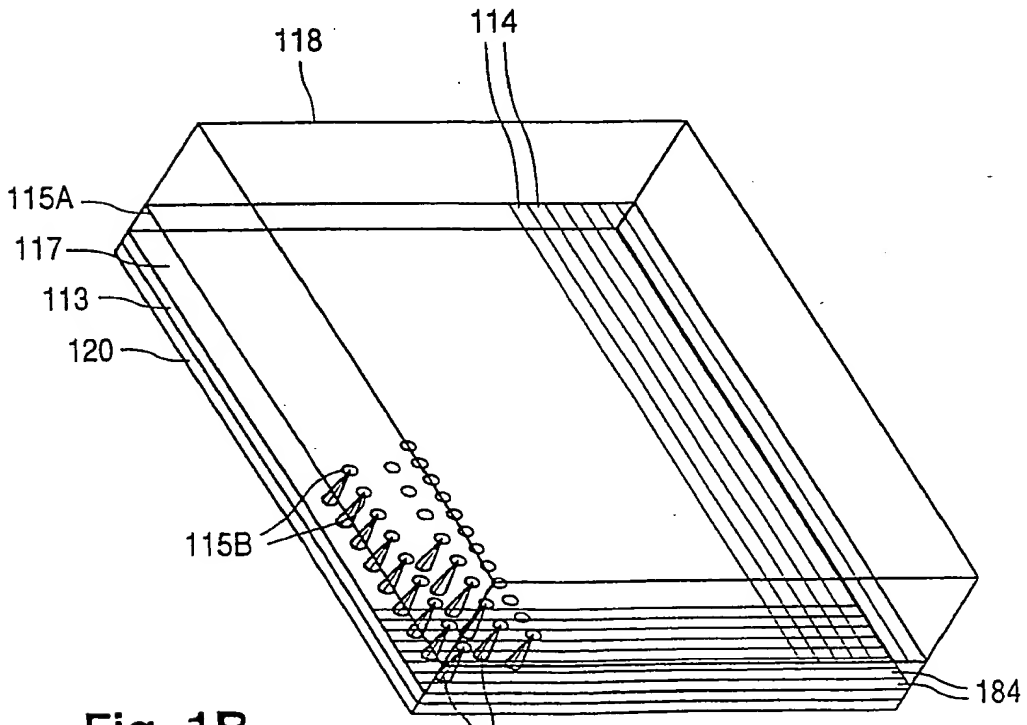

Fig. 1B
Prior Art

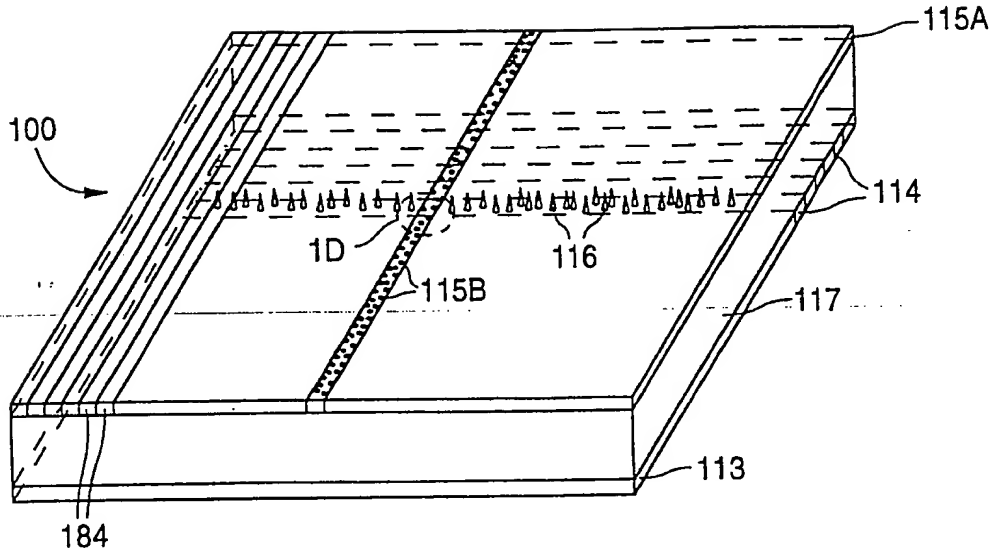

Fig. 1C
Prior Art

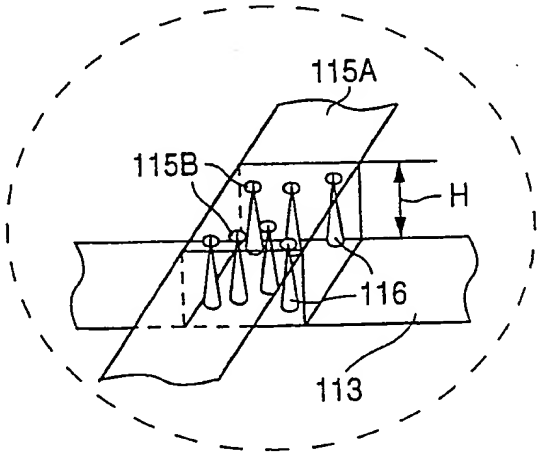

Fig. 1D
Prior Art

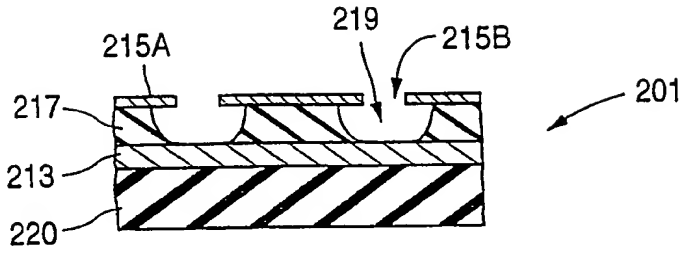

Fig. 2A

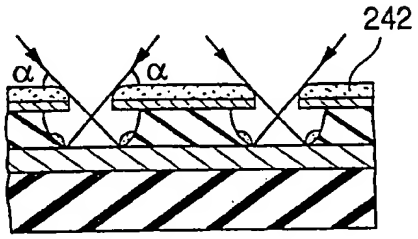

Fig. 2B

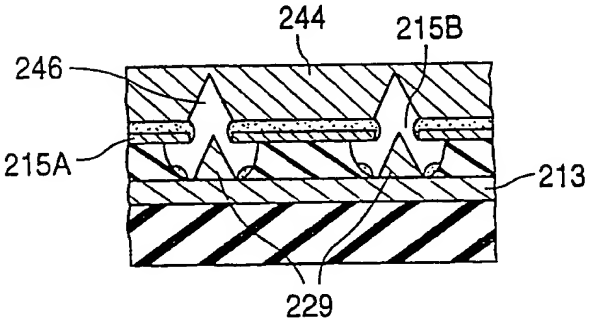

Fig. 2C

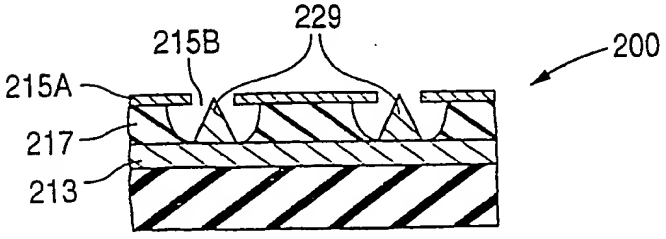

Fig. 2D

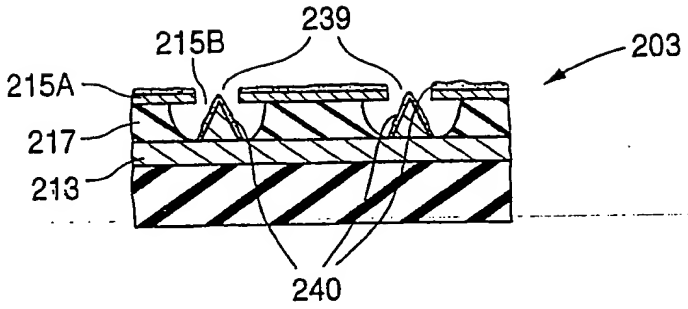

Fig. 2E

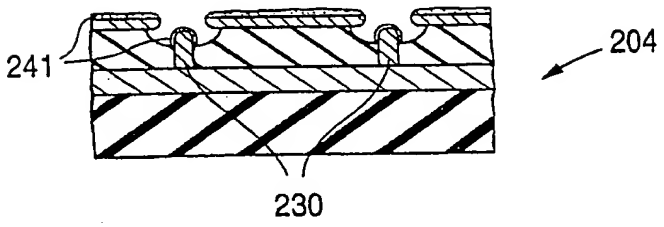

Fig. 2F

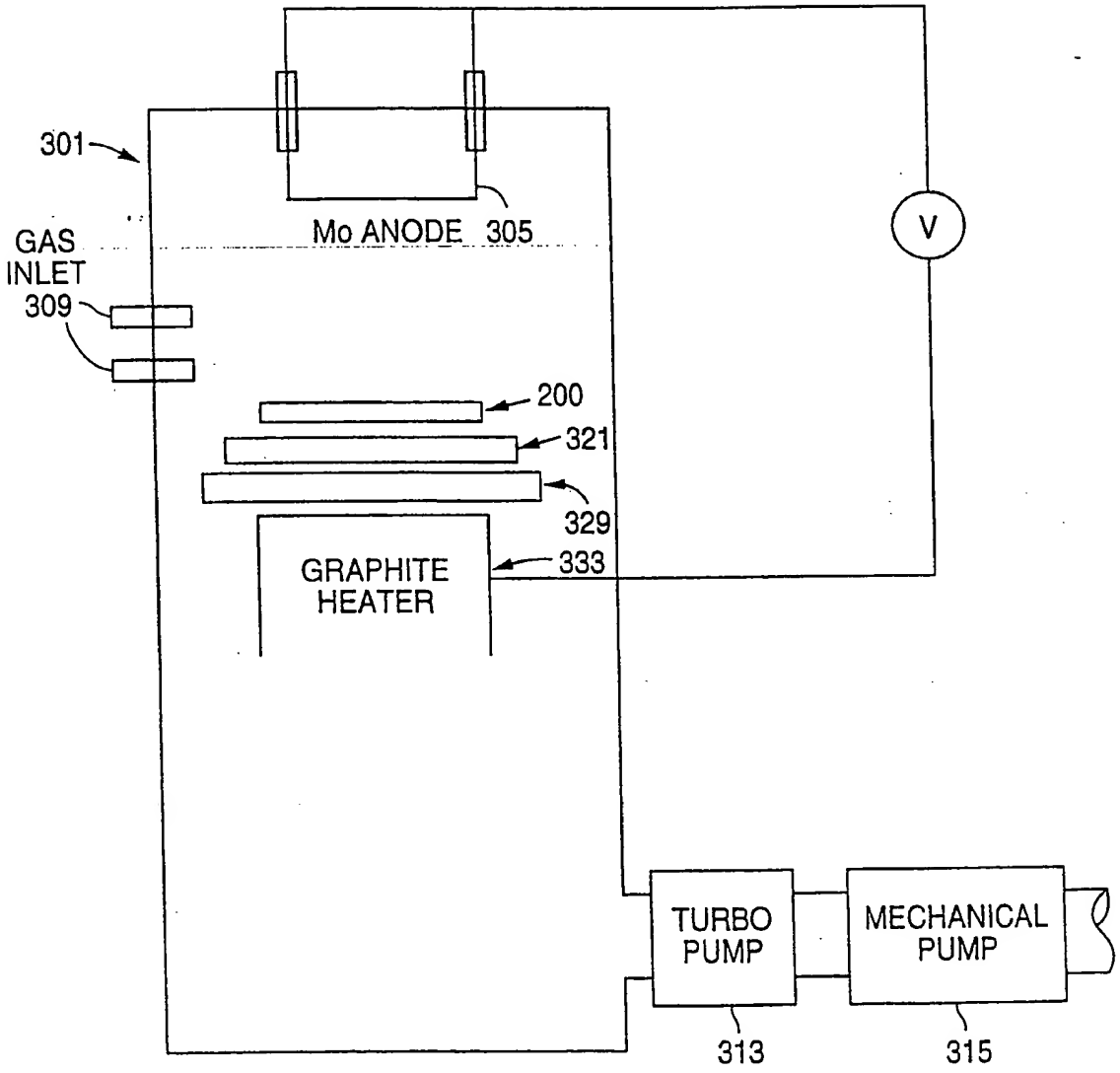
301
GAS
INLET
309
Mo ANODE 305
V
200
321
329
GRAPHITE
HEATER
333
TURBO
PUMP
MECHANICAL
PUMP
313
315

Fig. 3

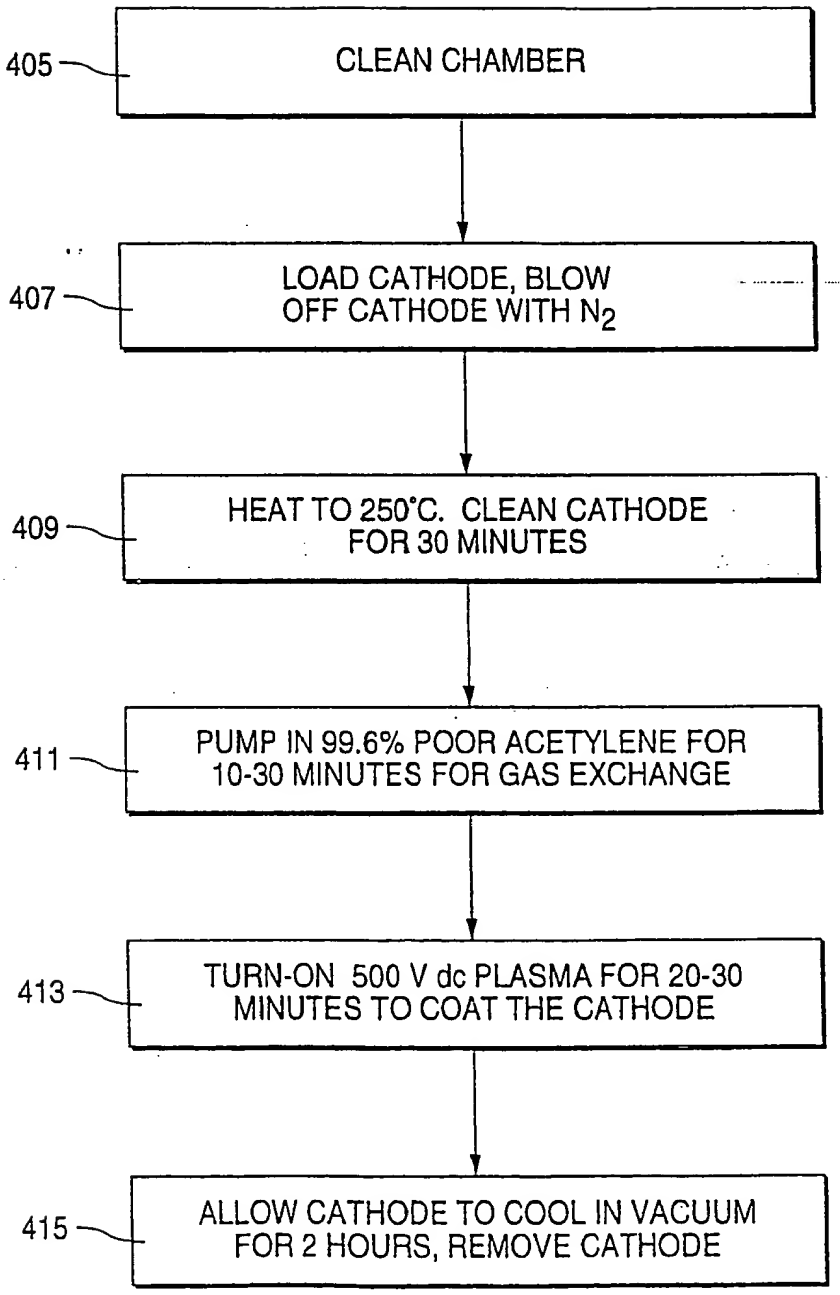
405
CLEAN CHAMBER
407
LOAD CATHODE, BLOW OFF CATHODE WITH N_2
409
HEAT TO 250°C. CLEAN CATHODE FOR 30 MINUTES
411
PUMP IN 99.6% POOR ACETYLENE FOR 10-30 MINUTES FOR GAS EXCHANGE
413
TURN-ON 500 V dc PLASMA FOR 20-30 MINUTES TO COAT THE CATHODE
415
ALLOW CATHODE TO COOL IN VACUUM FOR 2 HOURS, REMOVE CATHODE

Fig. 4

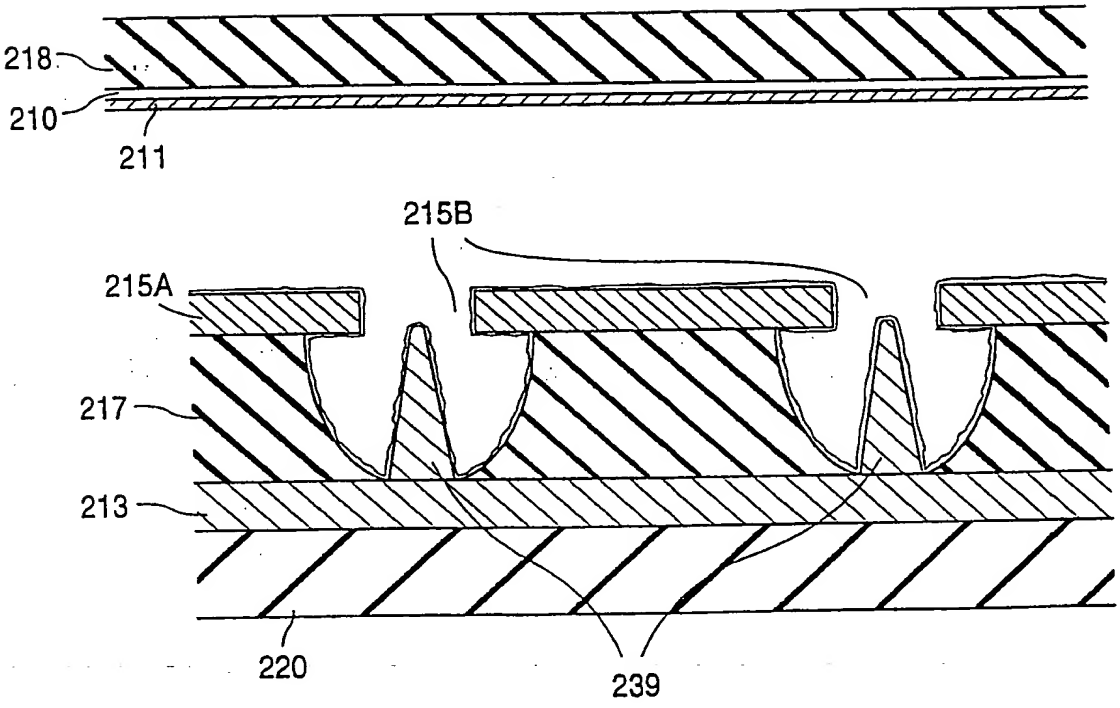

Fig. 5

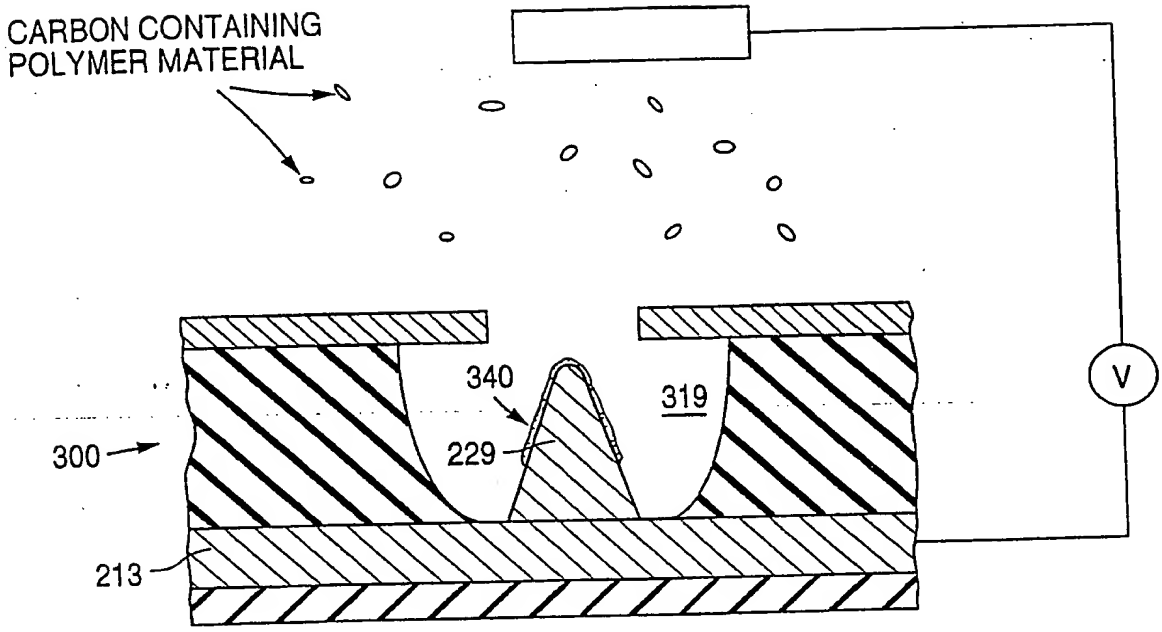

Fig. 6A

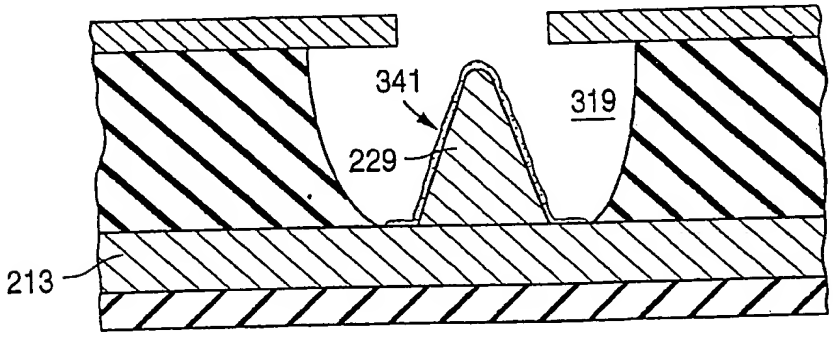

Fig. 6B

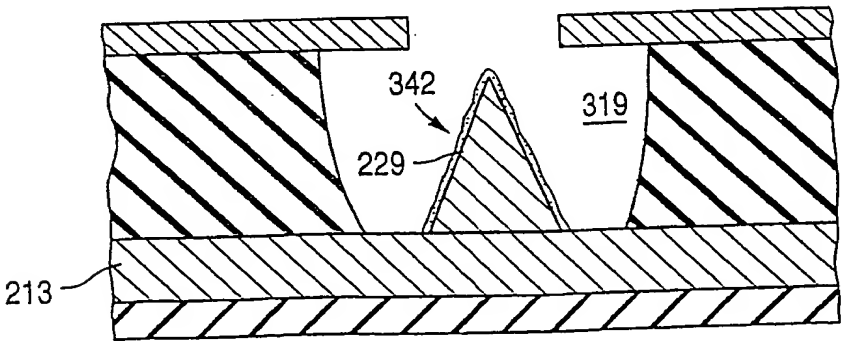

Fig. 6C

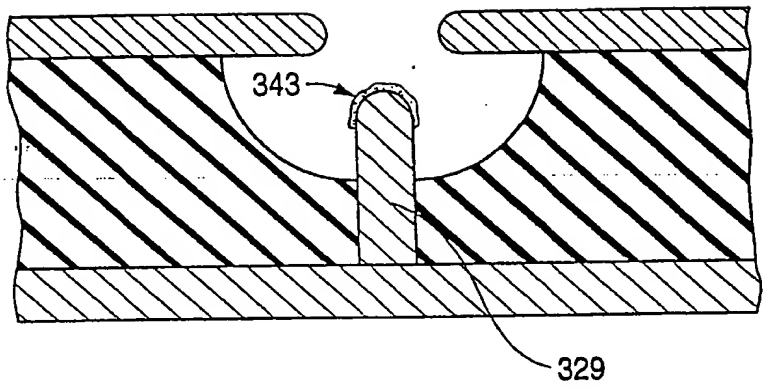

Fig. 6D

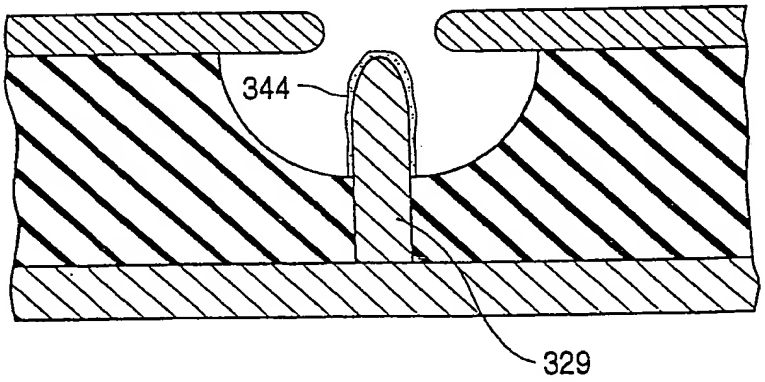

Fig. 6E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/03814

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01J 1/30, 19/24
US CL : 313/309, 336, 496; 445/50, 51
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 313/309, 351, 336, 495, 496, 497; 445/24, 50, 51, 60; 315/169.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,608,283A (TWICHELL et al.) 04 March 1997, (04/03/97) FIG. 2, col. 3, lines 6-28, col. 5, lines 55+.	1-3, 5, 7-9, 11, 13-17, 15-22, 26-23, 46, 47
X	US 5,469,014A (ITOH et al.) 21 November 1995, (21/11/95) FIG. 1, 2, Col. 3, lines 42-57, col. 4, lines 25-34.	1-4, 7, 8,14, 15-18, 20, 21
Y,P	US 5,697,827A (RABINOWITZ) 16 DECEMBER 1997, (16/12/97) FIG. 1, 15, col. 16, lines 62-64, col. 17, lines 4-15.	1, 3, 6, 7--13, 16, 23-29, 31-34, 36, 37, 41, 43, 48, 49
Y	US 5,463,271A (GEIS et al.) 31 OCTOBER 1995, (31/10/95) col. 2, line 64-col. 3, line 67, col. 9, line 41-56.	1, 3, 6, 7-9, 11, 16, 24, 27, 28

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
02 JUNE 1998

Date of mailing of the international search report
18 AUG 1998

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Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/03814

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,341,063A (KUMAR) 23 AUGUST 1994, (23/08/94) col. 2, lines 20-47, col. 4, lines 4+.	1, 3, 6, 10, 12, 13, 16, 23, 25-27, 28
Y	US 5,278,475A (JASKIE et al.) 11 JANUARY 1994, (11/01/94) FIG. 8, col. 5, lines 20-47.	2, 15
Y	MOUSA, M.S., et al. The Effects of Hydrogen and Acetylene Processing on Microfabricated Field Emitter Arrays, Applied Surface Science, 1993 (no month), vol. 67, pages 218-221.	34, 37, 41, 43, 49